



Patent  
Attorney's Docket No. 018656-232

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of ) MAIL STOP AF  
Kazunori Shionoya ) Group Art Unit: 2622  
Application No.: 09/824,836 ) Examiner: MARK R MILIA  
Filed: April 4, 2001 ) Confirmation No.: 1177  
For: MEMORY BOARD )  
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*Entered  
10/26/05  
JW*

**RESPONSE AFTER FINAL**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 30, 2005, the Examiner is respectfully requested to reconsider the application and withdraw the outstanding rejections.

Claims 1-9 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,535,368, hereinafter *Ho et al.* As argued in the response filed on February 16, 2005, the substance of which is incorporated herein by reference, *Ho et al.* does not disclose a memory board including a memory controller as well as a memory device. In response to the remarks filed on February 16, 2005, the Examiner indicated that "the Examiner understands" that the memory subsystem 10 illustrated in Figure 1 of *Ho et al.* is a "memory board" and as such the memory modules 12A and 12B can be connected to add additional memory capacity to the system. However, other than reciting the Examiner's understanding, the Examiner has provided no basis for the position that the memory subsystem 10 is a "printed wiring board" as recited in claims 1 and 7 or a "memory board" as recited in claim 4.